Design Guidelines for SAR Digital Receiver/Exciter Boards

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Abstract

High resolution radar systems generally require combining fast analog to digital converters and digital to analog converters with very high performance digital signal processing logic. These mixed analog and digital printed circuit boards present special challenges with respect to electromagnetic interference. This document first describes the mechanisms of interference on such boards then follows up with a discussion of prevention techniques and finally provides a checklist for designers to help avoid common mistakes.
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Foreword

The genesis of this work was the design of a series of digital receiver-exciter boards for radar. This report was intended to document the special considerations required for such designs.
1 Introduction

Synthetic Aperture Radar (SAR) and related modes such as Ground Moving Target Indicator (GMTI) rely on substantial coherent processing to extract signals from the noise. However, in addition to extracting the desired coherent signals, such processing also extracts undesired energies as well, such as those from frequency spurs, clock leakage, power supply switching noise, etc. This necessitates designing boards (e.g. parts layout, routing, and shielding) to provide exceptionally clean high-fidelity signals to any analog path components, including signal paths, power paths, and other reference signals.

The purpose of this document is to provide as much practical guidance as possible in a concentrated form. Section Error! Reference source not found. of this document describes a number of mechanisms whereby EMI can degrade radar performance. Section 3 describes techniques that have proven useful in high-signal integrity board designs. Section 4 provides a checklist of things that should be looked at when doing such a board design.

![Figure 1: Radar Digital Receiver-Exciter](image)

A typical implementation of the above block diagram is shown in Figure 2, Figure 3 and Figure 4. This board is a 3U cPCI board that contains both a 1200 Ms/s DRX and a 1200Ms/s DDS. The three blue coaxial jumpers carry the clock input, the DRX analog input and the DDS analog output. These jumpers are installed to bypass an optional RF processing stage.
Figure 2 DRX / DDS Assembly Front Side.

Figure 3 DRX / DDS Assembly Back Side.
Figure 4 DRX / DDS Assembly with Heat Sink/EMI Shield.
2 Mechanisms and Effects of EMI

2.1 Interferers

2.1.1 Digital Clocks and Signals

This kind of board often contains large amounts of digital logic running at an integer fraction of the sample rate, say $F_s/4$. In particular high speed converters often contain multiplexors and demultiplexors to reduce the data rate of the converters to something that FPGA’s can handle directly. The digital clocks and data of the converter can easily interfere with the sensitive analog clocks and data of those same converters.

Other common interferers are digital backplane busses such as PCI. 33.3MHz can nearly always be seen in the processed ADC data of digital receivers based on 33MHz PCI.

2.1.2 Switching Power Supplies

Power supplies can contain low frequency ripple from switching regulators usually in the range of 100KHz to 2 MHz. Synchronous digital logic and I/O can also modulate power supplies at the processing frequencies, usually several hundred megahertz.

Switching power supplies can also radiate quite a bit of energy due to the switching of inductive loads.

2.2 Victims

2.2.1 ADC Inputs

The ADC input is the most obvious victim signal on the board. EMI energy can be coupled into the traces that feed the ADC input and digitized along with the radar return signal. The digitizing stage is generally located after the de-ramp mixer so coherent tones can show up as bright spots in the radar image.

2.2.2 DAC Outputs

It is also possible to couple EMI energy onto the DAC output signal. Interference here is less serious than at the ADC input because the DAC output is generally running at the DAC full scale so the signal to interference ratio is maximized. Also, the transmit waveform is a linear FM chirp. Pure tone interference at this stage generally gets spread in de-ramp receive processing.
2.2.3 **Converter Sample Clocks**

The sample clocks for the ADC and DAC are perhaps the most sensitive signal on the digital receiver/exciter board. Interference on clocks generally shows up as frequency modulation of the carrier discussed in section 2.3.2.2.

2.2.4 **Converter Power Supplies and Reference Voltages**

Variation on ADC or DAC power supply pins can often amplitude modulate the carrier causing undesired double sideband spurs as discussed in section 2.3.2.1.

Additive energy from power supplies will also be a problem any time DC is in the transmit or receive information band. This is the case if quadrature synthesis is used to chirp right across DC. This would also be the case if the receive chain uses an analog quadrature demodulator to mix all the way to baseband. Receiver/exciter architectures that avoid DC have a big EMI advantage.

2.3 **Types of Interference**

Figure 5 shows a model of the various forms of interference that should be addressed in the design and verification of such a board. Additive interference is injected at the input along with the desired carrier. The carrier and additive interference is then amplitude and phase modulated by multiplicative interference mechanisms.

The model in Figure 5 is equally applicable to the transmit side. In that case a DAC replaces the ADC and the modulations occur in reverse order as shown in Figure 6.

![Figure 5: Receive EMI Model](image-url)
2.3.1 **Additive Interference**

Additive interference is when an unwanted signal simply adds to the desired carrier. If the interferer is truly additive the carrier can be turned off and the interference is still visible in the spectrum.

PCI clocks at 33.33MHz or 66.66MHz often show up as additive interference. Newer system interfaces such as PCI Express specifically address this problem by serializing and scrambling backplane signals.

Figure 7 below shows a carrier at 234.5MHz and an additive spur at 66MHz and 50dBc down. The noise floor is due to ideal quantization. The data was synthesized by a Matlab script adc_add.m which is included in section 7 of this document.
2.3.2 Multiplicative

Multiplicative interference requires the presence of a carrier in order to be seen because it does not add energy but rather modulates that carrier in some way. Multiplicative interference can cause amplitude modulation when it affects the gain of a converter. Multiplicative interference can cause phase modulation when it affects the sample time of the converter.

2.3.2.1 Amplitude Modulation

Figure 8 shows the spectrum of a carrier at 123.45MHz that is amplitude modulated by a 20 MHz sinusoid. Note the symmetric tones located 20MHz on either side of the carrier. This is the classic signature of AM interference. The data was synthesized by a Matlab script adc_am.m which is included in section 7 of this document.
2.3.2.2 Phase Modulation

When a periodic interferer contaminates the sample clock of a converter the effect is phase modulation. Phase modulation, like frequency modulation, causes frequency spurs evenly spaced by the frequency of the interferer. Figure 9 shows a carrier at 123.45MHz that is digitized by an ADC whose clock contains sinusoidal jitter at 20MHz.

In many cases it is necessary to use processing gain such as the coherent summing of many sample vectors in order to see the second and third phase modulation terms in the spectrum. In the example spectrum below phase deviation was set to 0.15 Unit Interval which is very heavy interference. The data was synthesized by a Matlab script adc_clock_pm.m which is included in section 7 of this document.
Figure 9: Example Spectrum with ADC Clock Jitter

Figure 10 shows the spectrum of data that contains additive, multiplicative AM and multiplicative FM interference. Generally when more than one interference mechanism is involved a forest of spurs will result making analysis difficult. For example, spurs caused by amplitude modulation can then be split again by phase modulation getting into the converter clock. Data for this plot was generated by adc_all.m in section Figure 10.
3 Techniques for EMI Mitigation on High-Speed Mixed Signal PCB’s

3.1 Simplify

Good signal integrity is easier to achieve when the board design is kept simple. Figure 1 on page 9 shows the block diagram for a typical digital receiver-exciter for radar applications. Necessary components are the high-speed digital to analog converter (DAC), high-speed analog to digital converter (ADC), a clock distribution network, an FPGA for digital processing and point of load power supplies.

High-speed analog I/O include the synthesized TX waveform, the high-speed sample clock and the receiver IF. These signals connect to the RF subsystem and must be carefully coupled onto the board and then extremely well protected.

As many as eight different non-standard power supply voltages may be required on such a board. Power conversion circuitry is often the messiest part of the design and care should be taken to isolate switching power supply noise from the high-speed analog I/O and from converter supply and reference pins.
3.2 Identify the most important signals

In terms of signal integrity, by far the four most important signals on the board are the ADC Clock, the ADC analog input, the DAC clock and the DAC analog output. Often just applying great care with these four signals will result in a receiver-exciter board with adequate performance for radar applications.

3.3 Use Good Design Practices for Digital Signals

This document assumes that good design practices are used for the digital portion of the board. Improper routing or termination can result in a digital signal that functions properly but radiates excessively. Good design practices include the following:

- Route over solid reference ground planes.
- Do not route signals over breaks or slots in the reference plane.
- Minimize trace lengths.
- Match trace lengths for high speed buses.
- Carefully design fanout pattern to escape BGA packages in fewer layers and with good signal integrity.
- Use controlled impedance, differential signalling where possible.
- Avoid wide digital busses.
- Turn down slew rates on digital outputs if possible.
- Select high performance BGA chip packaging.
- Correctly terminate high speed digital lines that require termination.
- Use on chip termination when available.
- Use appropriate power supply decoupling capacitors.

3.4 Provide Physical Separation for Sensitive Signal

Physical separation is the first line of defense for sensitive analog signals and clocks. The separation can be on the same layer and cross coupling falls off as 1/D^2 for parallel traces where D is the distance between traces. Even better is to separate sensitive signals onto different layers in the PCB stack up so that no agressor signals share the same reference planes with the signal to be protected.
3.4.1 Crosstalk Simulation Example

Figure 11 below shows a simple board layout imported into the Mentor Hyperlynx signal integrity simulator. The board was laid out in the Mentor PADS layout tool. A victim signal was created by connecting an LVDS driver to an LVDS receiver with a 3 inch 100 Ohm differential trace pair. A 100 Ohm differential termination resistor is placed at the receiver input. An aggressor signal was created by connecting a Xilinx CPLD 2.5V low voltage CMOS driver to the appropriate receiver via an unterminated single ended trace.

The LVDS victim traces are 5 mils wide and separated by 8.5 mils to maintain 100 Ohms impedance. The aggressor is also 5 mils wide and separated from the LVDS pair by 8.5 mils. The aggressor parallels the victim traces for 3 inches. All traces are on the same layer.

Figure 11 Hyperlynx layout for crosstalk testing

Figure 12 below shows the PCB stackup for the simulation. The victim and aggressor traces are all routed on layer 4. Layer 2 and layer 5 are both ground reference planes. All dielectric layers are 8 mils. This stackup is representative of a low density board but is useful for this analysis.
Figure 12 PCB stackup for Hyperlynx simulations.

Figure 13 below shows the Hyperlynx oscilloscope plot of the aggressor signal and the corresponding differential cross talk (LVDS+ - LVDS-) on the LVDS victim signal. Spacing between aggressor and victim is 8.5 mils. Figure 14 below shows a blow up of the same differential crosstalk. Note that this is a very severe case of crosstalk, approximately 180 mV peak-to-peak. For comparison, the National Semiconductor ADC08D1500 ADC has a full input range of 650mV p-p. This level of EMI on the this ADC input would be at -11 dBfs and the radar would not be useable.
Figure 13 Aggressor and victim waveforms for 8.5 mil gap

Figure 14 Blowup of differential crosstalk for 8.5 mil gap.
Now we rerun the simulation with the aggressor to victim gap increased to 20 mils. Figure 15 below shows the 30 mV p-p differential crosstalk with this spacing. If this crosstalk were imposed on the analog input of the ADC08D1500 ADC it would be at -26 dBfs, again not acceptable.

At this point we run into a limitation of the Hyperlynx simulator. It will only simulate crosstalk greater than 10 mV. 10 mV would only be down -36 dBfs with respect to the ADC input discussed earlier. We want more like -80 to -100 dBfs for a good radar digital receiver.

We know that crosstalk diminishes by 1/D² so we can plug in the numbers from the simulation to calculate the spacing we need between aggressor and victim. First let’s check that the two simulations we did are consistent. The two gap spacings were 8 mils and 20 mils. The two crosstalk values were 180 and 30 mV p-p. (1/8²)/(1/20²) = 6.25 ~ 180/30 = 6 so agreement is pretty good.

Now let’s calculate the spacing we need. 100 dBfs is 650 mV/10⁵ = 6.5uV. Extrapolating from the 20 mil gap (1/20²)/(1/D²) = 30E-3/6.5E-6 which gives D = 1360 mils or 1.3 inches!

Signal spacing requirements of over one inch are unheard in normal circuit design. Because of the enormous processing gain used in synthetic aperture radar, EMI levels around -100 dBfs are desireable. In this example, where traces are routed on the same layer, very large signal spacing is required to achieve those levels.
3.5 Balun coupling of high-speed I/O

The analog I/O and clocks of high speed converters use differential signalling in order to take advantage of its inherent common mode rejection. On the other hand, the RF connections for these signals are single ended shielded coax. To make the transition between single ended and differential signalling balun RF transformers should be used. Baluns are available in configurations that also provide galvanic isolation between the RF system and the digital receiver/exciter board. Baluns also provide AC coupling to allow biasing of the differential signal levels at the converter.

Sometimes it is not possible to place the RF connector close to the associated ADC or DAC I/O pins. In this case, because differential signalling is less sensitive to EMI than single ended routing, it is better to place the balun close to the connector and then run differential traces to the converter. This keeps the single ended 50 Ohm trace as short as possible.

Figure 16 shows one way to convert the 100 Ohm differential DAC analog output to 50 Ohms single ended using a 4:1 impedance ratio balun. The DAC output wants to see 100 Ohms differential so a 100 Ohm differential characteristic impedance transmission line is used to connect the DAC output to the balun. The balun in this picture has a 4:1 impedance ratio from its input to its output. Since the output of the balun is looking into a 50 Ohm line the input of the balun will look like 200 Ohms (4 x 50 Ohms). There needs to be 100 Ohms across the end of the the 100 Ohm transmission line in order to properly terminate it. The 200 Ohm resistor, R61, in parallel with the 200 Ohm balun input provides that 100 Ohm termination.

![Figure 16: Differential 100 Ohm to Single-Ended 50 Ohm Coupling of DAC Output with Balun](image)

Figure 17 shows one way to couple a 50 Ohm single ended RF signal into the 100 Ohm differential input of an ADC. High speed ADC chips generally have 100 Ohm differential termination built into the input on-die. It is customary to run 100 Ohm differential characteristic impedance transmission lines to the ADC input to take advantage of this on chip termination. T2 is a 1:4 impedance ratio balun with its low impedance side connected to 50 Ohms. This means that the output of the balun needs to see 200 Ohms.
The 50 Ohm resistors R192 and R191 match the 200 Ohm output impedance of the balun to the 100 Ohm impedance of the transmission line to the ADC input. Note that this same circuit can be used to couple the 50 Ohm single ended clock into the differential input of the board’s clock buffer.

Figure 17: Coupling a 50 Ohm Single Ended Signal into a 100 Ohm Differential Transmission line using a balun.

3.6 Fast Clock Buffers

Frequently a fanout buffer is used to distribute the sample clock from the STALO to the ADC and DAC chips as shown in Figure 1. The fan out buffer is one place where extra bandwidth can help improve signal integrity. The idea is that when the differential output of the fanout buffer swings the output spends a small amount of time near the crossover region between zero and one. While the differential output is in that region additive noise can affect the exact time of crossing and therefore modulate the sample clock.

A very fast clock fanout buffer will slew very quickly between states and therefore present less opportunity for clock modulation. The Micrel SY58020UMI 1:4 CML clock fan out buffer is an excellent example of such a fast buffer.

3.7 Analog Power Supply Ripple Isolation

3.7.1 Use ferrite beads to isolate supplies.

ADCs and DACs data sheets generally publish power supply rejection ratio specifications. For the National Semiconductor ADC08D1500 ADC chip the PSRR from \( V_A \) to the digitized input is 50 dB. This is very good performance for an 8 bit ADC but it means that 100mV p-p power supply ripple will show up as -66dBfs in the digitized data (full scale = 650mV p-p). Radar processing gain could easily make such a signal visible in the final image product.

Often converters have a \( V_{ref} \) input that has direct scaling relationship to the converter analog signal amplitude. Any ripple on the \( V_{ref} \) pin will amplitude modulate the
converter analog signal. An example is the REFIO pin of the MAX 19692 12 bit DAC. The voltage on REFIO is proportional to the DAC full scale output voltage.

Each analog power supply on a DAC or ADC should be routed through a ferrite and then decoupled well under the part. Power supplies may need to be decoupled from kilohertz to gigahertz. We have seen examples where receive processing creates a pulsed power supply load at the PRI rate (KHz) and this power supply modulation has shown up as an image artifact.

Figure 18 shows the kind of things that can be done to keep analog power supplies quiet. The top supply is a 3.3V analog supply to the DAC. The 3.3V backplane supply is specifically not used for this because of noise issues. Instead the 5V backplane supply is brought in through a ferrite bead to feed a linear regulator whose output is then filtered through a L-C-L “T” filter.

The bottom supply is a negative 5V analog supply for the MAX108 ADC. A switching inverter generates a -6V supply that feeds a -5V linear “clean up” regulator. Not shown on this schematic is another ferrite bead which is placed at the power pins of the ADC.

![Figure 18: Typical Power Supply Filtering](image)

Whenever possible shielded core inductors specifically designed to reduce EMI should be used in switching regulator designs.

### 3.7.2 Route power supplies instead of pouring.

For digital systems it is advantageous to pour large power planes to avoid routing power and to provide high frequency decoupling. For analog supplies big pours are vulnerable to capacitive coupling from other supplies and signals. It is considered good practice to
route analog supplies to small pours under the part where local decoupling caps are connected.

### 3.8 Shielding.

#### 3.8.1 Shield Plates and Cans

Often mixed signal board designs contain extensive shielding. Shield cavities can be incorporated into the cooling plate that is screwed down to the board. This plate would be designed to make contact with top surface of the hot parts for cooling but also make contact with exposed copper ground pours on the top layer of the board. These copper pours are tied to ground and form borders around major functional areas of the board. For example, the main 1.0V fpga power, the fpga, the DAC, the ADC, clock receiver are each isolated in their own cavities formed by the lid in contact with the pours. Ideally a lot of screw holes, say one per inch, are provided to maintain good contact between the plate and the board.

Another problem area for EMI is the coax connectors that connect to external RF systems. Often these connectors are through-hole PCB mount to provide sufficient mechanical integrity and stick out some distance from the back side of the board. As such they are susceptible to EMI from adjacent boards in the chassis. It is possible to design the PCB to accept shield cans that solder onto special shielding ground pads and prevent digital noise from entering sensitive analog I/O ports. See Figure 19 below.
3.8.2 Copper Pours

A common way to provide shielding is to place copper ground pours on the backside layer of the PCB. Usually the analog sections of the board do not require backside components or vias. This means that a nearly continuous copper pour can be made over the section of the board that contains the converter analog clocks and I/O.

Blind and buried vias need not penetrate to the the back side layer of the PCB. This means that nearly the entire back side of the board can be poured with copper. Then only back side and through hole components require breaks in the poured copper shield. The disadvantage of using special vias is a substantial increase in board fabrication cost.

3.8.3 Via Walls and Guard Traces

Low cost shielding can be applied around the sensitive analog clocks and I/O traces by using via walls. These are rows of vias attached to adjacent ground planes so that the protected signal is completely surrounded by ground. The vias can be stitched together with a guard trace.

The value of this technique over simple trace-to-trace separation is questionable. In some cases this technique is specified to guarantee that agressor signals are maintained a safe distance from the protected signal and so that layout designers recognize the special care needed with a particular signal.

3.9 Use more signal layers.

We used many more layers than necessary for routing so that signals such as the ADC data bus could run between a pair of ground planes. Also having a dedicated layer allowed those lines to be routed in the most direct (diagonal) path and not be constrained to north/south routing. Again, additional layer drive board cost so close communication with the board vendor is useful when designing the board stackup.

3.10 Use more ground layers.

Our high speed mixed signal receiver-exciters boards generally use about 6 ground layers to provide good signal integrity and shielding.

3.11 Rounding and Saturation

Historically some suspected signal integrity problems have turned out to be numerical errors in DSP firmware. Improper rouding can cause an unexpected DC bias in radar data. Lack of saturation logic can result in large discontinuities in the data due to two’s
complement wrapping. It is very important to use unbiased rounding and saturation at all points where word size must be reduced like at the output of a scaling accumulator.

### 3.12 Evaluate Completed Design

When a new digital receiver/exciter board design is completed it is important to go back and verify its performance by making a number of observations and measurements. Also sometimes when a new design is started a previous design is available for analysis. In that case the goal is to improve performance and avoid repeated mistakes.

#### 3.12.1 Observe DDS exciter output

The output of the synthesized linear FM chirp can be observed to look for additive and multiplicative interference.

![Figure 20 Typical setup for inspecting DDS output](image)

**Figure 20 Typical setup for inspecting DDS output**

#### 3.12.1.1 TX Off – Look for Additive Interference

First turn off the DDS output and look for additive spurs in the spectrum. Figure 21 below shows the spectrum at the output of the DDS with waveform synthesis turned off. Note the clock feed through at 300MHz. This DDS runs at a sample rate of 1200Ms/s and the DAC has a 2:1 input mux with a DDR clock running 300 MHz. Some energy at this frequency is almost unavoidable but in this case it is down nearly 80 dB from the carrier level.

Another clock is visible at exactly 200 MHz. It is difficult to guess the source of this interference. There is a 200MHz clock generated inside the FPGA as a reference to tune I/O delays. Also 200MHz could be the sixth harmonic of the 33.33MHz PCI bus clock. In any case, this tone is down 90 dB from the DDS output level.
3.12.1.2 CW on – Look for multiplicative spurs

By turning on the DDS output in continuous (non-pulsed) CW mode you can look for multiplicative EMI problems and excessive harmonic levels. Figure 22 below shows the DDS output set to 234.56789 MHz CW. You can see a number of spurs but the worst is about 70 dB down from the carrier.

In a finite resolution DAC the generated carrier will produce harmonics at every possible multiple of the carrier frequency. Also, the sample and hold is a sampled time device so harmonics beyond the Nyquist frequency will alias back into the Nyquist band of the DAC. This all makes interpreting spurs difficult.

These harmonics can cause artifacts in the computed SAR image. Because they are present in both the transmit and receive chirps these harmonics can de-chirp themselves and create false returns. These false returns will appear at integer multiples of range from scene center with respect to the true return. Such false returns are readily visible during delay line IPR testing.

Take a look at Figure 22 below. The carrier is labeled with marker 1 at 235 MHz. With a 600MHz span the marker frequencies are only accurate to 1 MHz. The second harmonic
has marker 2 at 469 MHz. The third harmonic would be at 704 MHz but it aliases back to 496 MHz. The fourth harmonic would be at 938 MHz but it aliases to 261 MHz. The following little Octave/Matlab script generates the aliased frequency of the first six harmonics.

```matlab
Fs=1200;
Fc=234.56789;
i=1:6;
harms = abs(mod(Fc*i+Fs/2,Fs)-Fs/2)
```

The resulting frequencies can all be seen in the spectrum analyzer plot.

<table>
<thead>
<tr>
<th>234.5679</th>
<th>469.1358</th>
<th>496.2963</th>
<th>261.7284</th>
<th>27.1606</th>
<th>207.4073</th>
</tr>
</thead>
</table>

![Spectrum of carrier with harmonics and multiplicative spurs](image)

3.12.1.3 Continuous Slow Chirp – Spurs in motion

A nice way to get a feel for how DDS spurs work is by setting the DDS into continuous mode but with a slow chirp rate. A chirp rate of one Nyquist bandwidth per minute.
allows you to watch the spurs move through the band of interest in real time. For this test it is necessary to set the sweep rate on the spectrum analyzer rather high so that the spur motion can be seen. Figure 23 below shows how the second and third harmonics move relative to the carrier. You can tell the order of the harmonic by the rate it moves. The second harmonic moves at twice the rate of the carrier. The third harmonic moves at three times the rate and so forth. In Figure 23 the third harmonic is larger than the second harmonic. That is apparent very quickly from watching the moving spectrum.

![Figure 23 Spectrum of slow moving carrier](image)

Finally, it is always important to measure Spur Free Dynamic Range (SFDR) for any DDS design. Figure 24 below shows SFDR for Sandia’s current DDS board plotted versus frequency. Section 7.5 contains the C++ code used to collect this data.

This program records the worst spur level and also the frequency of the worst spur. It is interesting to plot worst spur frequency versus carrier frequency in order to see which order of harmonic is limiting performance. In Figure 25 below it can be seen that during the upper half of the spectrum where SFDR is the worst performance is always limited by the third harmonic. Third harmonic problems can be caused by differential routing imbalance on the analog output between the DAC and the output balun.
Figure 24 DDS SFDR versus frequency.

Figure 25 Worst spur frequency versus carrier frequency.
3.12.2 Observe ADC input

The input of the ADC is driven by a circuit that includes 50 Ohm single ended routing, 100 Ohm differential routing, a balun and termination resistors. See Figure 17. These components form a network that can be affected by EMI but the 50 Ohm DRX input port is also an ideal place to observe EMI on the ADC input. Figure 26 below shows the setup for making these measurements. The 50 Ohm DRX input is just connected to the spectrum analyzer input.

Figure 26 Setup for observing EMI on ADC input.

Figure 27 below shows the spectrum measured from the DRX input port. Note there are coherent terms at 167MHz, 200MHz 267MHz, 300MHz and 333MHz all integer multiples of the 33.33 MHz PCI backplane clock used with this DRX. These spurs are a major disadvantage of synchronous parallel busses like PCI. The successor to PCI, PCI Express, contains a data scrambling feature built into the standard to address this problem.

In order to appreciate the amplitude of these spurs it is useful to compare them to the full scale ADC input range. A typical ADC for this type of application would be the ADC08D1500 which has a full scale input range of 650mV p-p differential = .24 dBm = 0 dBfs.

Looking at the spectrum in Figure 27 we see a spur is at 267MHz with a level of -90 dBm. There is 1 dB of loss in a typical balun and the coax cable to the spectrum analyzer probably has another 1 dB of loss. This means the 267 MHz spur level could actually be -88 dBm at the ADC input. This corresponds to about -88 dBfs relative to the full scale input amplitude of the ADC. Radar designers like to see -80 dBfs for interferers like this so this DRX should perform well in system.
There is another clock spur at 300MHz but this is something of a special case. Because the ADC DDR clock runs at that rate it is almost unavoidable to have a prominent spur there. Luckily 300MHz is one fourth of the sampling rate of the ADC and spurs at Fs/4 can generally be mitigated using pulse to pulse phase modulation techniques at the radar system level.

![Figure 27 Spectrum at ADC input - DDS running.](image)

### 3.12.3 Measure Return Loss at RF Ports

Return loss is defined as the ratio of energy sent into a port to the energy that reflects out of that same port. The greater the return loss the better. A perfect termination would have infinite return loss.

A network analyzer can be used to check the return loss into the clock inputs and analog receive ports. The purpose of making this measurement is to verify that good impedance matching has been achieved in the circuit. Return loss is dominated by the balun so the measured result should match published specs for the balun over the frequencies of interest.
Figure 28 Typical Clock Balun Return Loss

Figure 29 Typical balun for ADC or DAC analog I/O
Figure 30, Figure 31, Error! Reference source not found. below show the measurements made on a Sandia DRX / DDS board using the Agilent E8363B Network Analyzer.

For this board the clock runs at 1200 MHz and the return loss for that frequency is about 20 dB, pretty good. Over the ADC input frequency range, 175 to 425 MHz, Figure 31 shows we get better than 16 dB return loss.
Figure 31 Return loss at DRX input.
4 Design Checklist for High-Speed Mixed Signal PCB’s

This section is intended as a quick reference list of issues to consider.
- Review Previous Designs

- Simplify the Design
  - Minimize the number of chips
  - Minimize interfaces
  - Avoid wide busses
  - Minimize the number of supply voltages
  - Use On-Chip Termination

- Identify and Protect the four super critical signals
  - Provide physical isolation of critical signal from other signals.
  - Couple RF using baluns.
  - Use perfectly balanced routing.
  - Optimize impedance matching.

- High-Speed digital signals
  - Use appropriate reference planes.
  - Use matched length routing on high speed buses.
  - Use controlled impedance routing.
  - Use properly terminated lines.

- Filter and Decouple Power Supply Networks
  - Route and then locally pour power supply nets.
  - Use L-C filtering.
  - Use low ESR tantalum capacitors at supply.
  - Use broad spectrum chip capacitors at load.
- Shield
  - Use soldered shields on back side of RF connectors.
  - Consider pouring the entire back side as a grounded shield.

5 Summary and Conclusions

There are many advantages to combining radar digital receiver and exciter functions on the same module. Modern FPGA’s, DAC’s and ADC’s make this very practical. Nevertheless, combined DRX / DDS modules present special signal integrity challenges to circuit designers. Large amounts of digital processing and high speed digital interfaces in close proximity to sensitive analog signal require special care. This document describes the mechanisms involved, lists a variety of mitigation techniques to address those mechanisms and shows evaluation procedures that can be used to judge the final results.

In practice, when this level of care is taken, a digital receiver / exciter design for radar applications can be realized with adequate signal integrity performance on the first try.

6 List of Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
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<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
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<tr>
<td>AM</td>
<td>Amplitude Modulation</td>
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<tr>
<td>Balun</td>
<td>Balanced-Unbalanced – a passive impedance matching device similar to a transformer</td>
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<tr>
<td>dB</td>
<td>Decibel</td>
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<tr>
<td>dBc</td>
<td>Decibel relative to the carrier</td>
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<tr>
<td>dBfs</td>
<td>Decibels relative to full scale range of a device</td>
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<tr>
<td>dBm</td>
<td>Decibels relative to 1 miliwatt</td>
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<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
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<td>DDS</td>
<td>Direct Digital Synthesizer</td>
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<td>DRX</td>
<td>Digital Receiver</td>
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<tr>
<td>DSP</td>
<td>Digital Signal Processing</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>--------------------------------------------</td>
</tr>
<tr>
<td>EMI</td>
<td>ElectroMagnetic Interference</td>
</tr>
<tr>
<td>ESR</td>
<td>Effective Series Resistance</td>
</tr>
<tr>
<td>FM</td>
<td>Frequency Modulation</td>
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<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
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<tr>
<td>GMTI</td>
<td>Ground Moving Target Indicator</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
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<tr>
<td>IPR</td>
<td>ImPulse Response</td>
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<tr>
<td>I/O</td>
<td>Input Output</td>
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<tr>
<td>LO</td>
<td>Local Oscillator</td>
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<tr>
<td>mil</td>
<td>Milli-inch – 1thousandth of an inch</td>
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<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
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<tr>
<td>PCI</td>
<td>Peripheral Component Interconnect – a computer bus</td>
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<tr>
<td>p-p</td>
<td>Peak to Peak</td>
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<tr>
<td>SAR</td>
<td>Synthetic Aperture Radar</td>
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<tr>
<td>RF</td>
<td>Radio Frequency</td>
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<td>Receive</td>
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<td>S&amp;H</td>
<td>Sample and Hold</td>
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<tr>
<td>SFDR</td>
<td>Spur Free Dynamic Range</td>
</tr>
<tr>
<td>TX</td>
<td>Transmit</td>
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</table>

7 Appendix A – Matlab Code

7.1 Adc_add.m
% This program simulates additive EMI effects.
Badc = 8; % ADC word width.
N = 2^14;  % Number of ADC samples in simulation.
Fs = 1.0;  % Sampling rate.
Fc = round(.23456*N)/N;  % Carrier frequency with respect to sampling rate.
    % Force to integer number of cycles to avoid fft leakage.
EMI_dBc = -50; % amplitude of interferer relative to carrier.

Femi = .066666; % frequency of interferer.

% Calculate the vector of times when the ADC samples.
t = (0:N-1)/Fs;  
% Calculate emi.
s_emi = (10^(EMI_dBc/20))*sin(2*pi*t*Femi); 
% Form carrier with interference.
s = s_emi + sin(2*pi*t*Fc); 
% Quantize.
s = round((2^(Badc-1))*s)/2^(Badc-1); 

% Plot the resulting spectrum.
plot(Fs*(0:N-1)/N,20*log10(abs(fft(s.*hamming(N)'))));
title(sprintf('Amplitude Modulation of ADC Input: Fc=%2.3d, Fmod=%2.3d, Amod=%2.3d',Fc,Fmod,Amod));
ylabel('Amplitude (dB)');
xlabel('Normalized Frequency (f/Fs)');

7.2 Adc_am.m

% adc_am.m
% This program simulates amplitude modulation of the ADC analog input.
% This can occur if the reference voltage of the ADC has ripple on it.

Badc = 8; % ADC word width.
N = 2^14;  % Number of ADC samples in simulation.
Fs = 1.0;  % Sampling rate.
Fc = round(.12345*N)/N;  % Carrier frequency with respect to sampling rate.
    % Force to integer number of cycles to avoid fft leakage.
Fmod_am = .02; % frequency of amplitude modulation.
Amod_am = 1/100; % Magnitude of amplitude modulation of the carrier.

% Calculate the vector of times when the ADC samples.
t = (0:N-1)/Fs;  
% Calculate modulation signal.
s_mod = Amod_am*sin(2*pi*t*Fmod_am); 
% Form modulated carrier.
s = (1.0+s_mod).*(sin(2*pi*t*Fc)); 
% Quantize.
s = round((2^(Badc-1))*s)/2^(Badc-1); 

% Plot the resulting spectrum.
plot(Fs*(0:N-1)/N,20*log10(abs(fft(s.*hamming(N)'))));
title(sprintf('Amplitude Modulation of ADC Input: Fc=%2.3d, Fmod=%2.3d, Amod=%2.3d',Fc,Fmod,Amod));
ylabel('Amplitude (dB)');
xlabel('Normalized Frequency (f/Fs)');
7.3 Adc_clock_pm.m

% adc_clock_pm.m
% This program simulates phase modulation effects that occur when an interferer modulates an ADC clock.

 Badc = 8; % ADC word width.
 N = 2^14; % Number of ADC samples in simulation.
 Fs = 1.0; % Sampling rate.
 Fc = round(.12345*N)/N; % Carrier frequency with respect to sampling rate.
 Fmod = .02; % frequency of clock modulation.
 Amod = 1/15; % Magnitude of clock modulation in fraction of the sample period.

t_pure = (0:N-1)/Fs; % Calculate the vector of times when the ADC samples.
t_mod = (Amod/Fs)*sin(2*pi*(0:N-1)*Fmod/Fs);
t = t_pure+t_mod;

s_pure = sin(2*pi*Fc*t_pure);
s = sin(2*pi*Fc*t);
s = round((2^(Badc-1))*s)/2^(Badc-1); % Quantize.

plot(Fs*(0:N-1)/N,20*log10(abs(fft(s.*hamming(N))')));
title(sprintf('Sinusoidal Jitter on ADC Clock: Fc=%2.3d, Fmod=%2.3d',Fc,Fmod));
ylabel('Amplitude in dB');
xlabel('Normalized Frequency');

7.4 Adc_all.m

% adc_all.m
% This program simulates phase modulation, amplitude modulation and additive interference effects together.

 N = 2^14; % Number of ADC samples in simulation.
 Fs = 1.0; % Sampling rate.
 Badc = 8; % ADC word width.
 Fc = round(.34567*N)/N; % Carrier frequency with respect to sampling rate.
 Fmod_fm = .027; % frequency of clock modulation.
 Amod_fm = 1/20; % Magnitude of clock modulation in fraction of the sample period.
 Fmod_am = .013; % frequency of amplitude modulation.
 Amod_am = 1/100; % Magnitude of amplitude modulation of the carrier.
 Femi = .122; % frequency of interferer.
 EMI_dBc = -50; % amplitude of interferer relative to carrier.

t_pure = (0:N-1)/Fs; % Calculate the vector of times when the ADC samples.
t_mod = (Amod_fm/Fs)*sin(2*pi*(0:N-1)*Fmod_fm/Fs);
t = t_pure + t_mod;

s_emi = (10^(EMI_dBc/20))*sin(2*pi*t*Femi); % Calculate emi.

s = s_emi + sin(2*pi*t*Fc); % Form carrier with interference.

s_mod_am = Amod_am*sin(2*pi*t*Fmod_am); % Calculate amplitude modulation signal.

s = (1.0 + s_mod_am).*s; % Form modulated carrier.

s = round((2^(Badc-1))*s)/2^(Badc-1); % Quantize.

plot(Fs*(0:N-1)/N,20*log10(abs(fft(s.*hamming(N))')));

7.5 Sfdr_plot.cpp

#include <stdio.h>
#include <stdlib.h>
#include <unistd.h>
#include <math.h>
#include <time.h>
#include <string>
#include <sstream>
#include <utility>
#include <map>
#include <vector>
#include <iostream>
#include <complex>
#include <assert.h>
#include "ComboBoard.h"
#include "GPIB.h"

using namespace ComboBoard;

typedef std::complex<double> dcomplex;

namespace {
  const double FACTOR = 1.0;
  const double LO_freq_Hz = 3.3e9 * FACTOR;
  GPIB sa("spectrum");
  typedef std::map<std::pair<int16_t, int16_t>, double> ec_cache_t;
  ec_cache_t ec_cache;
}

void startup() {
  reset();

  DDS::set_tx_chirp_params(0, 0, 0);
  DDS::set_tx_chirp_deltas(0, 0, 0);
  DDS::set_rx_chirp_deltas(0, 0, 0);
DDS::DDS_Control dds_control;
dds_control.AEC_Enable = false;
dds_control.QEC_Enable = false;
dds_control.DC_Correction_Enable = false;
dds_control.write();

sa.write("*IDN?\n");
fprintf(stderr, "Using Spectrum Analyzer: %s", sa.read().c_str());
sa.write("*RST;*CLS\n");
sa.write(":DISP:MENU:STAT off\n");
sa.write(":INIT:CONT off\n");
sa.write(":*FREQ:CENT 300 MHz;SPAN 600 MHz;:BAND 100 kHz\n");
sa.write(":*DISP:WIND:TRAC:Y:RLEV 0 dBm;*WAI\n");
usleep(100000);
}

void shutdown() {
    //TAC::set_tac_enable(false, false);
    sa.write("*RST;*CLS\n");
    sa.write(":*INIT:CONT on\n");
}

void set_freq(double freq_Hz) {
    TAC::set_tac_enable(false, false);
    DDS::set_tx_chirp_params(0, freq_Hz*M_PI/600e6, 0);
    DDS::set_rx_chirp_params(0, freq_Hz*M_PI/600e6, 0);
    TAC::set_tac_enable(true, true);
    usleep(300);
}

// This function uses marker 2 to read the 2nd biggest tone in the
// spectrum.
// It goes to the max peak then to Next Peak. It keeps looking for
// Next Peak until if finds one at least 3MHz from the carrier to avoid
// false readings on the side of the carrier tone.
void get_sa_spur_dBm(double* amp, double* freq, double Fcarrier) {
    sa.write(":*INIT:IMM;*OPC?\n");
    sa.read();
    sa.write(":*CALC:MARK2:MAX;*WAI\n");
    std::istringstream ss;
    double peak_dBm, peak_freq;
    do {
        sa.write(":*CALC:MARK2:MAX:NEXT;*WAI\n");
        sa.write(":*INIT:IMM;*OPC?\n");
        sa.read();
        sa.write(":*CALC:MARK2:Y?\n");
        ss.str(sa.read());
        ss >> peak_dBm;
        *amp = peak_dBm;
        sa.write(":*CALC:MARK2:X?\n");
        ss.str(sa.read());
        ss >> peak_freq;
        *freq = peak_freq;
    } while (abs(peak_freq-Fcarrier) < 3e6);
}
// This function reads the peak value and its frequency from the SA.
void get_sa_peak_dBm(double* amp, double* freq) {
  sa.write(":\INIT:IMM;*OPC?");
  sa.read();
  sa.write(":\CALC:MARK1:MAX;*WAI");
  sa.write(":\INIT:IMM;*OPC?");
  sa.read();

  // Read amplitude of peak in dBm.
  sa.write(":\CALC:MARK1:Y?");
  double peak_dBm;
  std::istringstream ss(sa.read());
  ss >> peak_dBm;
  *amp = peak_dBm;

  // Read frequency of peak.
  sa.write(":\CALC:MARK1:X?");
  double peak_freq;
  ss.str(sa.read());
  ss >> peak_freq;
  *freq = peak_freq;
}

int main(int argc, char **argv) {
  double peak_dbm, peak_freq, spur_dbm, spur_freq;
  startup();

  const int Npoints = 199;
  const double Fnyq = 600e6;
  for(int i=0;i<Npoints;i++){
    double Fcarrier = (i+0.5)*Fnyq/double(Npoints);
    set_freq(Fcarrier);

    usleep(100000);
    get_sa_peak_dBm(&peak_dbm, &peak_freq);
    get_sa_spur_dBm(&spur_dbm, &spur_freq, Fcarrier);
    fprintf(stdout, "%f  %f  %f  %f  %f  %f\n", Fcarrier, peak_dbm, peak_freq, spur_dbm, spur_freq, peak_dbm-spur_dbm);
  }

  //shutdown();
}

8 References


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## Distribution

Unlimited Release

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